Please amend Claim 16 as follows:

16. (Thrice amended) A method for fabricating a semiconductor device with a trenched gate comprising:

forming an oxide layer on the surface of a semiconductor substrate;

forming a nitride layer on said oxide layer;

etching a trench having substantially upright vertical sidewalls and a bottom surface in said semiconductor substrate;

forming a trench-to-gate insulating layer inside the trench, wherein the trench-to-gate insulating layer comprises a trench gate dielectric spacer formed on the upright vertical sidewalls inside the trench and a trench gate tunneling dielectric formed on the bottom surface inside the trench;

forming a trenched gate electrode on the trench-to-gate insulating layer inside the trench;

forming a source region and a drain region in the semiconductor substrate such that the source and drain regions partially extend laterally underneath the bottom of the trench;

forming sidewall dopings on the sidewalls to reduce coupling between the control gate and the source and drain regions;

forming an inter-gate dielectric layer on a top surface of the trenched gate electrode; and

forming a control gate electrode on a top surface of the inter-gate dielectric layer.

Please amend Claim 19 as follows:

19. (Thrice amended) A method for fabricating a semiconductor device with a trenched gate comprising:

etching a trench having substantially upright vertical sidewalls and a bottom surface in a semiconductor substrate;

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forming a trench-to-gate insulating layer inside the trench, wherein the trench-to-gate insulating layer comprises a trench gate dielectric spacer formed on the upright vertical sidewalls inside the trench and a trench gate tunneling dielectric formed on the bottom surface inside the trench;

forming a trenched gate electrode on the trench-to-gate insulating layer inside the trench;

forming a source region and a drain region in the semiconductor substrate such that the source and drain regions partially extend laterally underneath the bottom of the trench;

forming an inter-gate dielectric layer on a top surface of the trenched gate electrode;

forming a control gate electrode on a top surface of the inter-gate dielectric layer, and

wherein the step of forming a source region and a drain region comprises corner-limiting diffusion process.